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Amendments to the Claims

Claims 1-5 have been previously cancelled. Please cancel Claim 23 and amend the remaining Claims as follows:

1-5. (Canceled)

6. (Original) A method for fabricating a semiconductor device, comprising:

forming an interlayer insulating film on a semiconductor substrate that exposes lower wiring and a lower insulating film;

selectively etching the interlayer insulating film to form a first electrode opening that exposes the lower wiring;

forming a first electrode in the first electrode opening so that the first electrode opening is filled;

selectively etching the interlayer insulating film at a region adjacent to the first electrode to form a second electrode opening;

forming a dielectric layer along inner walls that define the second electrode opening;

forming a second electrode on the dielectric layer to fill the second electrode opening; and

forming upper wiring on at least a portion of the second electrode.

7. (Original) The method of claim 6, wherein, following the filling of the first electrode opening with the first electrode, the first electrode is formed by performing chemical

mechanical polishing of a material used for the first electrode until the interlayer insulating film is exposed.

8. (Original) The method of claim 6, wherein following the filling of the second electrode opening with the second electrode, the second electrode is formed by performing chemical mechanical polishing of a material used for the second electrode until the interlayer insulating film and the first electrode are exposed.

9. (Original) The method of claim 8, wherein the dielectric layer on the first electrode and the interlayer insulating film is removed when performing chemical mechanical polishing to form the second electrode.

10. (Original) The method of claim 6, wherein the upper wiring is formed by forming an upper insulating film over the first electrode, the dielectric layer, the second electrode, and the interlayer insulating film, selectively etching the upper insulating film to form a wiring opening that exposes at least a portion of the second electrode, and filling the wiring opening with a metal material.

11. (Original) The method of claim 6, wherein the dielectric layer is formed by layering silicon oxide and silicon nitride.

12. (Original) The method of claim 6, wherein the first electrode and the second electrode are each formed to have a plurality of branches that extend from a base portion.

13. (Currently Amended) A method for fabricating a semiconductor device, comprising:

forming an interlayer insulating film having a first trench (a first electrode opening) on a substrate;

forming a first electrode of a capacitor within the first trench;

forming a second trench (a second electrode opening) in the interlayer insulating film adjacent to the first electrode to expose a side of the first electrode;

forming a dielectric layer along inner walls of the second trench; and

forming a second electrode of the capacitor on the dielectric layer to fill the second trench, including the steps of (i) forming a second metal layer on the interlayer insulating film to fill the second trench, and (ii) performing chemical mechanical polishing of the second metal layer until a surface of the interlayer insulating film is exposed.

14. (Previously Presented) The method of claim 13, wherein each of the first and second electrodes has a top view in shape of a comb having a plurality of recess and concave patterns.

15. (Previously Presented) The method of claim 14, wherein the recess patterns of the first electrode are formed face to face with the concave patterns of the second electrode, and the concave patterns of the first electrode are formed face to face with the recess patterns of the second electrode.

16. (Previously Presented) The method of claim 13, wherein the first and second electrodes have walls facing each other, each wall having the plurality of recess and concave patterns.

17. (Previously Presented) The method of claim 16, wherein the recess patterns of the first electrode are formed face to face with the concave patterns of the second electrode, and the concave patterns of the first electrode are formed face to face with the recess patterns of the second electrode.

18. (Previously Presented) The method of claim 13, wherein the dielectric layer is formed in a multi-layered structure having at least two layers.

19. (Previously Presented) The method of claim 13, wherein the dielectric layer includes a silicon oxide layer and a nitride layer.

20. (Previously Presented) The method of claim 13, wherein the first and second electrodes are formed on the same layer.

21. (Previously Presented) The method of claim 13, wherein the first and second electrodes are made of copper.

22. (Previously Presented) The method of claim 13, wherein the step of forming the first electrode includes

forming a first metal layer on the interlayer insulating film to fill the first trench; and

performing chemical mechanical polishing of the first metal layer until a surface of the interlayer insulating film is exposed.

23. (Cancelled)

24. (Previously Presented) A method for fabricating a semiconductor device, comprising:

forming a lower insulating layer having a wire opening on a substrate;

forming a lower wire within the wire opening;

forming an interlayer insulating film on the substrate including the lower insulating layer and the lower wire;

forming a first electrode opening in the interlayer insulating film to expose the lower wire;

forming a first electrode of a capacitor within the first electrode opening to contact the lower wire;

forming a second electrode opening in the interlayer insulating film adjacent to the first electrode to expose a side of the first electrode;

forming a dielectric layer along inner walls of the second electrode opening;

forming a second electrode of the capacitor within the second electrode opening; and

forming an upper wire electrically connected with the second electrode.

25. (Previously Presented) The method of claim 24, wherein each of the first and second electrodes has a top view in shape of a comb having a plurality of recess and concave patterns.

26. (Previously Presented) The method of claim 25, wherein the recess patterns of the first electrode are formed face to face with the concave patterns of the second electrode, and the concave patterns of the first electrode are formed face to face with the recess patterns of the second electrode.

27. (Previously Presented) The method of claim 24, wherein the first and second electrodes have walls facing each other, each wall having the plurality of recess and concave patterns.

28. (Previously Presented) The method of claim 27, wherein the recess patterns of the first electrode are formed face to face with the concave patterns of the second electrode, and the concave patterns of the first electrode are formed face to face with the recess patterns of the second electrode.

29. (Previously Presented) The method of claim 24, wherein the dielectric layer is formed in a multi-layered structure having at least two layers.

30. (Previously Presented) The method of claim 24, wherein the dielectric layer includes a silicon oxide layer and a nitride layer.

31. (Previously Presented) The method of claim 24, wherein the dielectric layer is formed at both sides and a lower surface of the second electrode.

32. (Previously Presented) The method of claim 24, wherein the first electrode is formed on the lower wire.

33. (Previously Presented) The method of claim 24, wherein the first electrode is formed on the lower wire and the lower insulating layer adjacent to the lower wire.

34. (Previously Presented) The method of claim 24, wherein the second electrode is formed on the lower insulating layer.

35. (Previously Presented) The method of claim 24, wherein the second electrode is formed on the lower wire and the lower insulating layer.

36. (Previously Presented) The method of claim 24, wherein the first and second electrodes are formed on the same layer.

37. (Previously Presented) The method of claim 24, wherein the first and second electrodes are made of copper.

38. (Previously Presented) The method of claim 24, wherein the step of forming the lower wire includes

forming a metal layer on the lower insulating layer to fill the lower wire opening; and

performing chemical mechanical polishing of the metal layer until a surface of the lower insulating layer is exposed.

39. (Previously Presented) The method of claim 24, wherein the step of forming the first electrode includes

forming a metal layer on the interlayer insulating film to fill the first electrode opening; and

performing chemical mechanical polishing of the metal layer until a surface of the interlayer insulating film is exposed.

40. (Previously Presented) The method of claim 24, wherein the step of forming the second electrode includes

forming a metal layer on the interlayer insulating film to fill the second electrode opening; and

performing chemical mechanical polishing of the metal layer until a surface of the interlayer insulating film is exposed.